In the Claims

Amend claims 6 and 10 and add new claims 14-20 as follows:

1. (Original) Data transmission system having a plurality of Local Area Networks (LANs) interconnected by a hub including a plurality of LAN adapters respectively connected to the plurality of LANs, the data transmission system comprising:

> a packet switch interconnecting the plurality of LAN adapters, wherein a packet transmitted by a first LAN adapter to the packet switch includes a header containing at least an address of a second LAN adapter to which the packet is forwarded, the packet switch which includes a plurality of N x N identical packet switch modules, each of the packet switch modules being associated with m input ports and m output ports having a rank selector which is hardwired to provide a rank k from 0 to N-1 to each column of N modules corresponding to the same output ports, the rank being provided to all memory blocks of the column in order to shift the physical address of each output port in the column by an offset of k x m, the input and output ports both being respectively connected to the plurality of LAN adapters, each pair of input port and output port defining a cross point at which is located a memory block for storing a data packet received from the input port corresponding to the cross point and which is to be forwarded to the output port corresponding to the cross point.

2. (Original) Data transmission system according to claim 1, wherein the memory block comprises a data memory unit for storing at least a data packet, a header validation control block for determining whether the header of a data packet received from the input port contains the address of the output port associated with the cross point, and a memory controller for storing the data packet into the data memory unit if the header contains the address of the output port and for reading the data packet to forward the data packet to the output port.

3. (Original) Data transmission system according to claim 2, wherein a scheduler is associated with each output port, the scheduler selecting at each clock time a memory block among all memory blocks corresponding to the output port and causing the memory block to forward the data

packet stored in the data memory unit to the output port when predetermined criteria are met.

4. (Original) Data transmission system according to claim 1, further comprising an input control block connected to each input port for buffering a data packet received from said input port before transmitting said data packet over a distributed data bus connected to all memory blocks corresponding to said input port, said input control block including an input memory unit for buffering said data packet received from said input port and a first memory controller for storing said data packet into said input memory unit and reading said data packet to forward it over said distributed data bus.

5. (Original) Data transmission system according to claim 4, wherein said input control block further includes a multiplexer for selecting either the output of said input memory unit or directly the bus connected to said input port when said input control block is not a first switch module of said packet switch.

6. (Currently Amended) Data transmission system according to claim 1, wherein ~~each~~ a down stream switch module among said N x N identical packet switch modules includes for each output port an input expansion data block for buffering a data packet received from an expansion bus in connected to an up stream switch module and corresponding to the same output port as said output port of said down stream switch module.

7. (Currently Amended) Data transmission system according to claim 6, wherein said input expansion data block includes an expansion memory unit for buffering said data packet received from said expansion bus in and a second memory controller for storing said data packet into said expansion memory unit and reading said expansion memory unit to forward it to said output port of said down stream switch module.

8. (Original) Data transmission system according to claim 3, further comprising a back-pressure mechanism which sends back-pressure signals to input adapters for requesting the input adapters to reduce the flow of the data packets transmitted to said packet switch when there is too much

overflow detected by one or several schedulers of one of said switch modules.

9. (Original) Data transmission system according to claim 8, further comprising an overflow mechanism which receives overflow control signals from the schedulers of said packet switch when there is too much overflow and transmits an overflow signal to said back-pressure mechanism.

10. (Currently Amended) Data transmission system having a plurality of Local Area Networks (LANs) interconnected by a hub including a plurality of LAN adapters respectively connected to the plurality of LANs, the data transmission system comprising:

a packet switch interconnecting the plurality of LAN adapters, wherein a packet transmitted by a first LAN adapter to the packet switch includes a header containing at least an address of a second LAN adapter to which the packet is forwarded, the packet switch which includes a plurality of N x N identical packet switch modules, each of the packet switch modules being associated with m input ports and m output ports having a rank selector which is hardwired to provide a rank k from 0 to N-1 to each column of N modules corresponding to the same output ports, the rank being provided to all memory blocks of the column in order to shift the physical address of each output port in the column by an offset of k x m, the input and output ports both being respectively connected to the plurality of LAN adapters, each pair of input port and output port defining a cross point at which is located a memory block for storing a data packet received from the input port corresponding to the cross point and which is to be forwarded to the output port corresponding to the cross point,

wherein the memory block comprises a data memory unit for storing at least a data packet, a header validation control block for determining whether the header of a data packet received from the input port contains the address of the output port associated with the cross point, and a memory controller for storing the data packet into the data memory unit if the header contains the address of the output port and for reading the data packet to

forward the data packet to the output port;

a scheduler associated with each output port, the scheduler selecting at each clock time a memory block among all memory blocks corresponding to the output port and causing the memory block to forward the data packet stored in the data memory unit to the output port when predetermined criteria are met; and

an overflow mechanism which receives overflow control signals from the schedulers of said packet switch when there is too much overflow and transmits an overflow signal to said back-pressure mechanism,

~~Data transmission system according to claim 9,~~ wherein said back-pressure mechanism receives overflow control signals from a right adjacent switch module and from a bottom adjacent switch module.

11. (Original) Data transmission system according to claim 10, wherein said back-pressure mechanism informs said overflow mechanism which alerts the corresponding schedulers and requests the corresponding schedulers to decrease the transmission of the data packets when said overflow mechanism receives overflow control signals from the bottom adjacent switch module.

12. (Original) Data transmission system according to claim 11, wherein said back-pressure mechanism alerts the input adapters of the corresponding switch module and requests the input adapters to decrease the transmission of the data packets when said back-pressure mechanism receives overflow control signals from the right adjacent switch module.

13. (Original) Data transmission system according to claim 1, wherein said header of the data packet includes two bytes in which the first byte contains an identification field (unicast, multicast) and the second byte contains a module address field when said packet switch comprises several packet switch modules.

14. (New) Data transmission system having a plurality of Local Area Networks (LANs) interconnected by a hub including a plurality of LAN adapters respectively connected to the plurality of LANs, the data transmission system comprising:

a packet switch interconnecting the plurality of LAN adapters, wherein a packet transmitted by a first LAN adapter to the packet switch includes a header containing at least an address of a second LAN adapter to which the packet is forwarded, the packet switch which includes a plurality of N x N identical packet switch modules, each of the packet switch modules being associated with m input ports and m output ports having a rank selector which is hardwired to provide a rank k from 0 to N-1 to each column of N modules corresponding to the same output ports, the rank being provided to all memory blocks of the column in order to shift the physical address of each output port in the column by an offset of k x m, the input and output ports both being respectively connected to the plurality of LAN adapters, each pair of input port and output port defining a cross point at which is located a memory block for storing a data packet received from the input port corresponding to the cross point and which is to be forwarded to the output port corresponding to the cross point,

wherein each down stream switch module among said N x N identical packet switch modules includes for each output port an input expansion data block for buffering a data packet received from an expansion bus in connected to an up stream switch module and corresponding to the same output port as said output port of said down stream switch module.

15. (New) Data transmission system according to claim 14, wherein the memory block comprises a data memory unit for storing at least a data packet, a header validation control block for determining whether the header of a data packet received from the input port contains the address of the output port associated with the cross point, and a memory controller for storing the data packet into the data memory unit if the header contains the address of the output port and for reading the data packet to forward the data packet to the output port.

16. (New) Data transmission system according to claim 15. wherein a scheduler is associated with each output port, the scheduler selecting at each clock time a memory block among all memory blocks corresponding to the output port and causing the memory block to forward the data packet stored in the data memory unit to the output port when predetermined criteria are met.

17. (New) Data transmission system according to claim 14. wherein said input expansion data block includes an expansion memory unit for buffering said data packet received from said expansion bus in and a second memory controller for storing said data packet into said expansion memory unit and reading said expansion memory unit to forward it to said output port of said down stream switch module.

18. (New) Data transmission system according to claim 14, further comprising a back-pressure mechanism which sends back-pressure signals to input adapters for requesting the input adapters to reduce the flow of the data packets transmitted to said packet switch when there is too much overflow detected by one or several schedulers of one of said switch modules.

19. (New) Data transmission system according to claim 18, further comprising an overflow mechanism which receives overflow control signals from the schedulers of said packet switch when there is too much overflow and transmits an overflow signal to said back-pressure mechanism.

20. (New) Data transmission system according to claim 14, wherein said header of the data packet includes two bytes in which the first byte contains an identification field (unicast, multicast) and the second byte contains a module address field when said packet switch comprises several packet switch modules.